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Design and fabrication of a micro fuel cell array with "flip-flop" interconnection

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Abstract

A design configuration is presented for integrated series connection of polymer electrolyte fuel cells in a planar array. The design is particularly favorable for miniature fuel cells and has been prototyped using a variety of etch and deposition techniques adopted from microfabrication. The series path is oriented in a "flip-flop" configuration, presenting the unique advantage of a fully continuous electrolyte requiring absolutely no interconnecting bridges across or around the membrane. Electrical interconnections are made by thin-film metal layers that coat etched flow channels patterned on an insulating substrate. Both two-cell and four-cell prototypes have successfully demonstrated the expected additive performance of the integrated series, and peak power in a four-cell silicon assembly with hydrogen and oxygen has exceeded 40 mW/cm^2. Factorial experimentation has been applied to investigate the adequacy of metal film conduction over etched topology, and results conclude that film thickness dominates over other design parameters. The design effort and subsequent testing has uncovered new topics for extended study, including the possibility of lateral ionic conduction within the membrane as well as the effects of non-uniform reactant distribution.

Keywords: Micro fuel cell; Series interconnection; Micromachining

1. Introduction

The application of fuel cells to portable power is motivated by numerous factors including high power density and high energy-to-weight ratio [1]. A fundamental advantage over batteries is the decoupling of the energy converter (membrane, catalyst and electrodes) and energy storage (typically a hydrogen-based fuel). This decoupling allows the fixed cell components and the refillable fuel to be customized independently for load requirements as well as convenience.

Miniaturizing fuel cells for portable applications, however, is not simply a matter of reducing physical dimensions. Rather, new designs and manufacturing approaches must be employed, especially because macro-sized fuel cell components are limited by characteristic fabrication constraints. The machining of flow structures, for example, is constrained by the brittleness of graphite, and molding is limited in deep narrow channels. Furthermore, as the raw size of an engineering product becomes smaller, it becomes more essential to manufacture units in batch, parallel or continuous processes because piecewise treatment becomes economically prohibitive. Therefore, processes such as photolithography, etching and vapor deposition may be more appropriate than cutting, molding, fastening, etc. The production of integrated-circuit chips is a particularly strong example that takes advantage of parallel fabrication. Given such considerations, adaptation of micromachining processes has provided a welcome avenue for developing fuel cells in small dimensions and for observing scaling effects [2,3].

The voltage of a single cell is fixed by its particular electrochemical reaction, so it is necessary to connect several cells in series to obtain higher voltage. Most conventional fuel cells are combined into stacks in a *back-to-back* orientation, and often an electrically conductive bipolar plate makes the series connection between neighboring cells (Fig. 1). In contrast, a few approaches explore advantages of *side-by-side* configurations in which the cells are connected in a lateral direction [4,5]. Such a form factor

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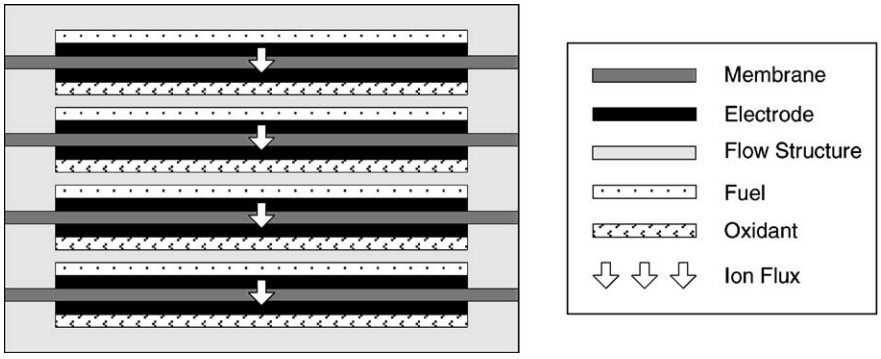

Fig. 1. Conventional bipolar fuel cell stack. Series connection is made by arranging unit cells back-to-back with an electrically conductive separator plate.

would be favored over a conventional stack assembly, for applications, such as flat-panel displays, personal digital assistants and wearable computers. One manifestation of the side-by-side configuration is the ''banded membrane'' concept (Fig. 2, upper diagram) in which the electrodes overlap such that cathode of one cell straps across the membrane to the anode of the next adjacent cell [6]. Such construction even shows promise for better volumetric packaging compared to conventional vertical stacks in low-power applications [7].

A limitation of most planar arrangements, however, is that interconnections must ultimately cross from one side of the membrane to the other. These cross-membrane interconnections can be made at the outer perimeter of a cell array by ''edge-tabs'' [8], or by routing breaches through the central area of the membrane. Interconnection at the perimeter limits design flexibility and may require longer conductor length, thereby increasing resistive losses. Breach interconnection through the membrane presents an extremely difficult challenge with respect to local sealing, and the problem is particularly severe for polymer electrolytes that may deform grossly according to humidity level. In response to such challenges, earlier work by the present authors has proposed a new concept of laterally interconnecting cells in a ''flip-flop'' configuration [9]. Such a configuration uses one-sided bipolar films and thereby eliminates the need to ever cross the membrane plane. This paper validates actual performance and discusses practical design considerations.

2. Design features

The characteristic feature of the flip-flop configuration is the interconnection of electrodes from two different cells on the *same side* of the membrane, as shown in Fig. 2. Fig. 3 shows a more extended three-dimensional layout for 16 cells. Although wafer-based devices are not so amenable to stacking a large number of layers, in principle multiple layers of interconnected cells can of course be stacked vertically to achieve greater flexibility with respect to form factor. There are numerous technical advantages beyond the essential benefit of low-profile design, as articulated below.

2.1. Fully continuous membrane

One of the most unique aspects of plane-separated interconnection is that the sandwiched membrane can be perfectly continuous. As Fig. 3 shows, not only is the membrane free of any breaches, but also it is never necessary for interconnect components to cross it—not even around the perimeter. Geometrically the membrane is a plain continuous sheet with no special shape constraints, so its processing and handling are very straightforward.

2.2. Single-level interconnects

A fundamental difference between any horizontally arrayed configuration versus a vertically stacked arrangement is that there must be a clear distinction between

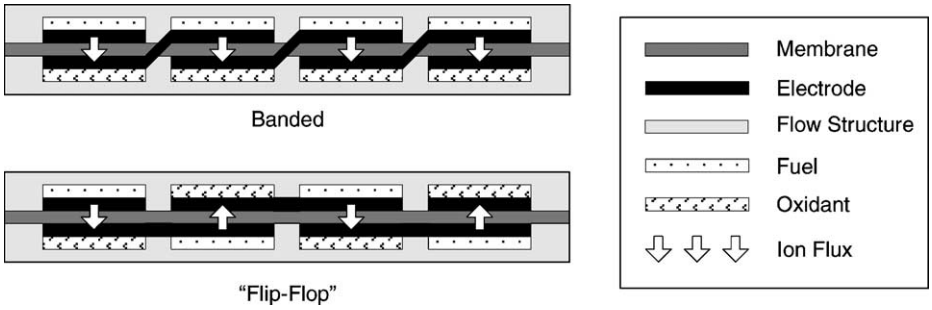

Fig. 2. ''Flip-flop'' planar series interconnection. In contrast to the banded configuration, the flip-flop scheme has single-level interconnects that never cross the membrane plane.

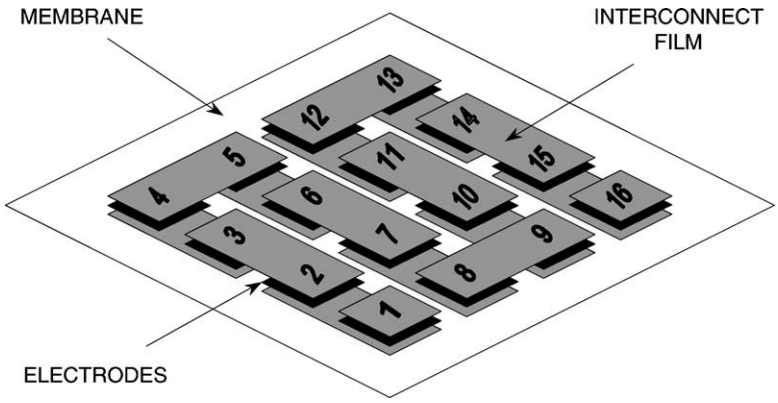

Fig. 3. Sixteen-cell layout with flip-flop series interconnection. The numbering of the cells indicates the series path, with end terminals at cells 1 and 16. The upper level connections between cells 6 and 7 as well as cells 10 and 11 require no communication with the perimeter.

electrically conducting and insulating regions. Otherwise all cells would be connected in parallel rather than meeting the objective of serial interconnection. This prevents the use of a single material, such as graphite or metal, and the electronically conducting regions must be selectively arranged. The flip-flop design is particularly well suited to address this need. Processing is relatively simple because all electronically conductive paths are treated on a single level with no need for vias, tabs or other three-dimensional features. The in-plane complexity and resolution become almost limitless, considering the ease by which metal patterns can be created using photolithography and selective etching or deposition.

2.3. Low-resistance conductor paths

It is important to re-emphasize that this design does not require that electronically conductive paths travel to the outer perimeter of the cell array in order to be interconnected. In Fig. 3, for example, all 16 cells are arranged in series, even though the electrode connections at the top side of cells 6 and 7, and 10 and 11 have no communication with the perimeter. An advantage is that it is possible to arrange interconnects such that all have wide width and short length. This is preferred over a system having thin, meandering metal traces which would result in higher electrical resistance. Furthermore, it is possible to have a very large number of densely packed cells without the undesirable condition of having to ''wire'' centrally located cells with a complex network of electrical traces.

2.4. One-sided terminal access

Also evident in Fig. 3 is the fact that there is single-sided access to both end terminals, in contrast to most fuel cells which have end terminations on opposite sides of the membrane. Having both electrical terminals easily accessible from the top side of the assembly offers flexibility for system-level design and integration. Applications may include surface-mount technology (SMT) for on-board connection to active electronic devices.

2.5. Sealing

One clear disadvantage of flip-flop interconnection is that reactant chambers must alternate between fuel and oxidant. While this may be a prohibitive condition for large fuel cells, there may be suitable solutions in micro-scale because of numerous wafer-level packaging strategies, such as anodic bonding. These methods are intended for making highly reliable hermetic seals for a multitude of unit cavities per substrate. While some approaches like silicon fusion bonding are strictly constrained to high temperature, numerous strategies for low temperature bonding are also being developed [10–12].

3. Experimental

Multiple prototype units were fabricated to verify basic performance and also to explore issues related to the microfabrication approach. The most simple case of a two-cell series was produced using glass substrates, followed by a four-cell version in silicon. Neither processing strategy is wholly superior to the other, but each offers unique advantages. Wet etching, as used in the glass prototype, lends well to batch processing and offers low capital investment. Dry etching, as used in the silicon version, has the capability to produce finer features with much higher aspect ratio.

3.1. Prototype construction

Prototype development focused on the microfabrication of flow structures using techniques adopted from silicon and glass micromachining. The membrane, catalyst and electrode materials were obtained commercially for repeatable performance. Specifically, these membrane–electrode assemblies (MEAs) consisted of Nafion® 115 with carbon cloth backing and 0.4 mg/cm^2 carbon-supported platinum. Custom alignment of multiple electrode pairs onto a single membrane was coordinated with the supplier (BCS Technology, Byran, TX).

Although brittle, glass and silicon substrates were chosen for initial prototyping to take advantage of well-characterized processes adopted from bulk micromachining. However, in broader perspective etching is certainly applicable to polymers, metals and other substrates as well. Furthermore, complex geometric structures can be pattern-transferred to a variety of alternative materials using a micromachined master [13] for further design flexibility.

A simple rectangular array of island pillars was selected for flow distribution behind each electrode. Such an open pattern is favorable for reducing flow resistance considering the small device size, and the simple grid layout has demonstrated fair performance compared to other channel configurations [14]. Inlets and outlets were arranged at diagonally opposite corners, as a method of obtaining adequate uniformity with minimal complexity [15]. Although not within the scope of the present study, a wide variety of alternative flow-field designs may also be implemented with the same principle of photo-patterning and etching. A gold film was patterned onto flow structures by physical vapor deposition to define conductive regions and to form the interconnections among cells.

3.1.1. Two-cell assembly in wet-etched glass

The most basic implementation of the flip-flop design consists of only two cells, as shown in Fig. 4. A common conductive member interconnects the two cells by linking the cathode of the first cell with the anode of the second. The figure also shows a photograph of the upper flow structure formed by etching channels in glass. The overall area of each cell is 5 cm^2 (22 mm × 22 mm), and the channels were approximately 150 μm deep. The flow distribution pillars are 400 μm wide and arranged in a uniform rectangular grid with 400 μm spacing.

The cavities of the flow structure were patterned by wet etching a glass substrate. The substrate was a borofloat glass wafer having 100 mm diameter and 680 μm thickness. A 150 nm film of amorphous silicon deposited by low-pressure chemical vapor deposition (LPCVD) served as the etch mask. The etch openings were created by plasma etching with SF_6 and C_2ClF_5 through the pattern defined by a photoresist layer. The actual wet etching of the channels in glass was achieved using concentrated hydrofluoric acid (49% HF). Etch rate with agitation was approximately 7 μm/min, and 5 min etch/rinse cycles were used to prevent redeposition of material. Electrically conductive regions were patterned on the surface by sputtering gold through an overlay stencil. The thickness of the gold was measured by stylus profilometry to be approximately 170–200 nm.

3.1.2. Four-cell assembly in dry-etched silicon

A four-cell assembly in silicon explored a greater number of cells with more complex interconnection. This prototype also demonstrated further miniaturization by packing all four cells (now 10 mm × 10 mm) in an area similar to the footprint of one cell from the glass prototype. A total of 16 cell regions were fabricated simultaneously on a single silicon wafer, as shown in Fig. 5. The wafer was subsequently diced such that one wafer provided two complete four-cell assemblies. The flow chambers were etched 200 μm deep and the square distribution pillars were 100 μm × 100 μm in size, arranged in a uniform rectangular array 100 μm apart. Cross-channels etched on different planar levels of the wafer provided proper gas routing to alternate fuel and oxidant chambers in a ‘‘checker-board’’ arrangement.

The flow structures were fabricated from a silicon wafer substrate, 100 mm in diameter and typically 500 μm thick. Dry etching was performed using a STS Multiplex ICP

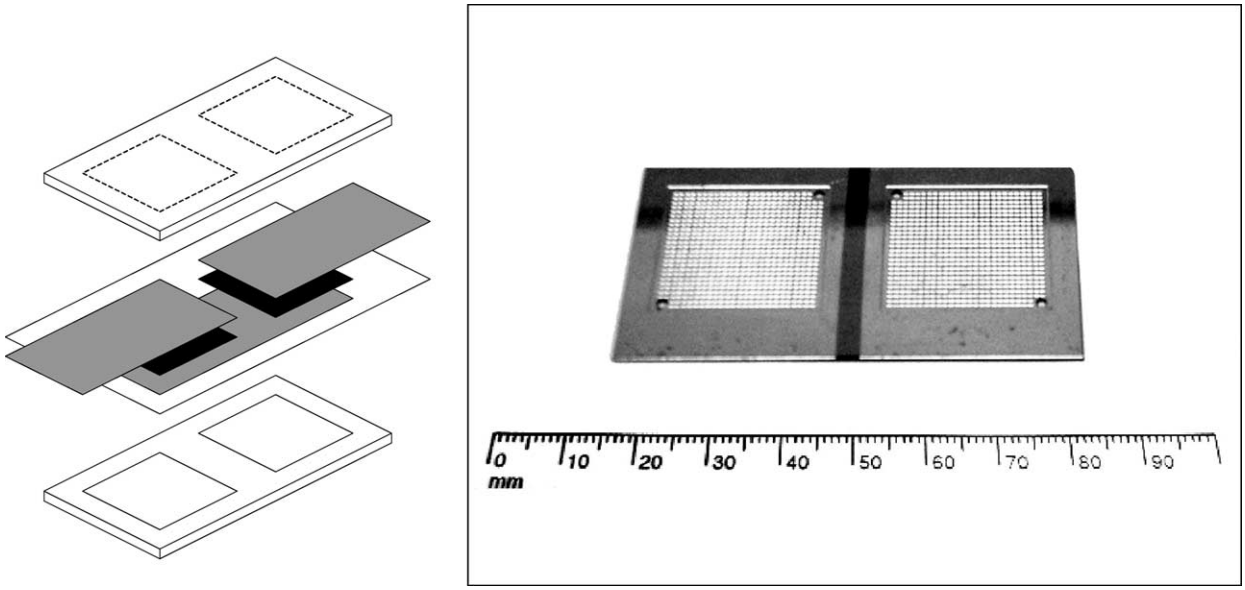

Fig. 4. Two-cell assembly. The interconnection between the two cells is made by a conductive film that spans across the lower electrode side of both cells.

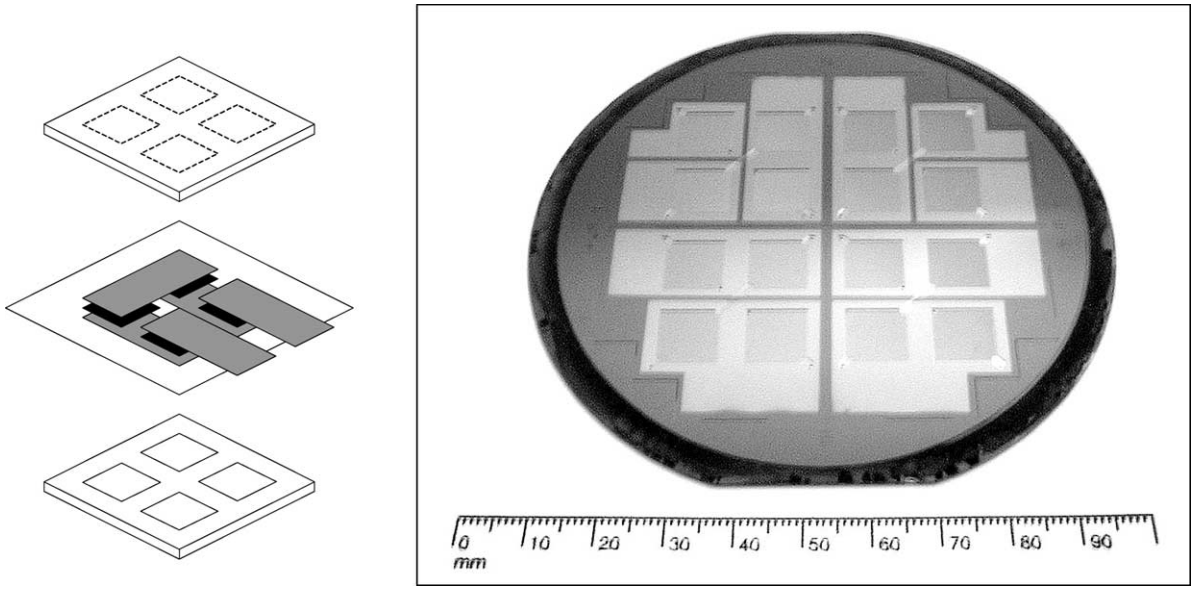

Fig. 5. Four-cell assembly. Sixteen cell regions (four sets of four) are simultaneously etched in a silicon wafer, followed by selective patterning of electrically conductive regions to appropriately form the series interconnections.

Deep Reactive Ion Etcher, with an inductively coupled plasma at 13.56 MHz, coil rf power 600 W, and electrode rf power 120 W. The etchant gas was SF_6 (130 sccm, 36 mT) and intermittent passivation with C_4F_8 (85 sccm, 18 mT) enabled vertical sidewall profiles. Etch rate was naturally geometry-dependent, but typically 2–3 μm/min. A thin silicon dioxide layer was added to the etched silicon surface by thermal oxide growth in a tube furnace. Electrically conductive areas were then defined by depositing metal films onto the oxide surface through a silicon shadowmask stencil. A 100 nm gold layer was deposited in an Innotec electron beam evaporation chamber, preceded by a 15 nm chromium layer just beneath the gold to promote adhesion. The insulating oxide was necessary to avoid inadvertent deposition laterally over the topological features, which was observed to cause partial short-circuiting in early prototypes. The directional nature of evaporation was found to be superior to sputtering, with respect to maintaining well-defined boundaries between conducting and insulating regions. Fig. 6 shows a close-up image of the pillar features, and Fig. 7 highlights key steps in the fabrication sequence.

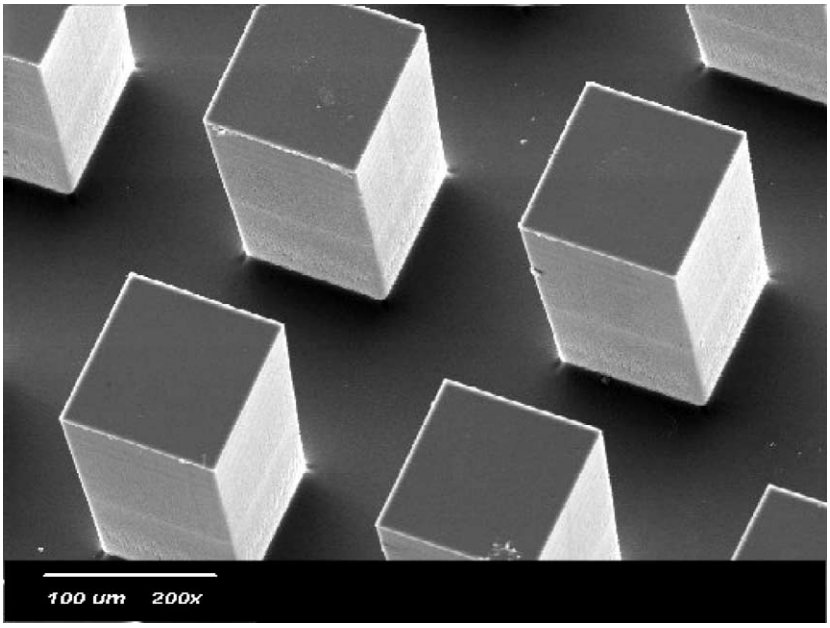

Fig. 6. Flow distribution pillars etched in silicon. The deep reactive ion etching process produces fine-resolution features with straight vertical sidewalls and high aspect ratio. The surface is selectively coated with a gold film to define conductive regions.

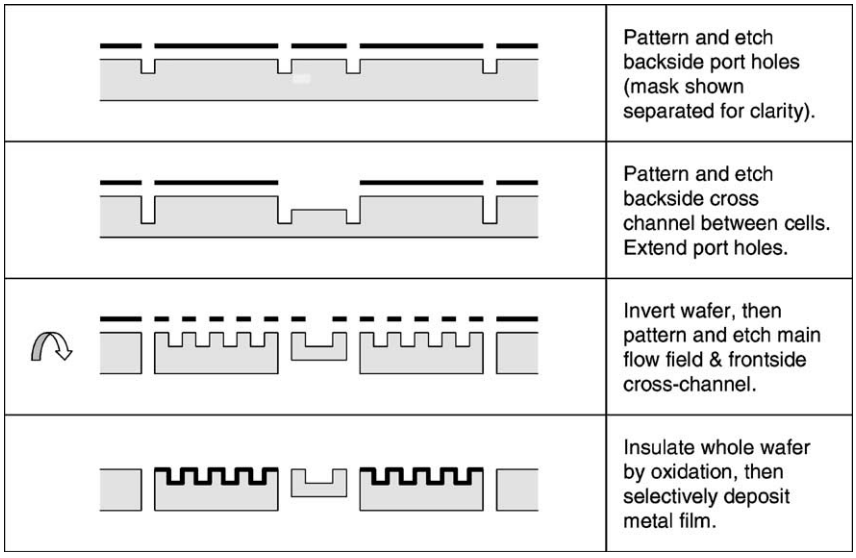

Fig. 7. Silicon multi-cell etch sequence. Flow fields for multiple cells on a single substrate are etched in a three-level sequence using both front and back sides of a silicon wafer. Gas cross-channels as well electrical series connections are created as integrated parts of the overall design.

3.2. Test conditions

The flow channels were pressed onto the MEAs by supplementary backing plates to interface gas fittings. Thin silicone rubber gaskets provided sealing between the substrates and the backing plates, as well as around the periphery of each electrode. The entire assembly was assembled using only hand-tightened fasteners with the minimum force required to provide adequate sealing without over-compression. Hermetic sealing was confirmed by pressurizing and isolating the system while monitoring leak rate at an inline pressure gauge. Electrical contact points were arranged to allow voltage measurement arbitrarily between any pair of electrodes, thereby enabling comparison of individual cells versus the overall series assembly.

Compressed hydrogen and oxygen gases were used as the fuel and oxidant, respectively. The gases were delivered under back-pressure regulation, inlet monitored at 35 kPa for two-cell experiments and 100 kPa for four-cell runs (gage pressure). Measurements were acquired using a Gamry PC4/750 potentiostat system interfaced to a laboratory computer. Cell performance was allowed to stabilize approximately 30 min before measurements were recorded, but no external heating was applied.

4. Results and discussion

4.1. Performance validation

The first objective of the experimental trials was simply to verify that flip-flop interconnection does in fact exhibit the additive result from each of its unit cells. This was proven for both the two-cell and four-cell configurations. These initial tests led to observations of further topics, such as lateral cross-conduction and flow uniformity, as discussed below.

4.1.1. Two-cell assembly

The polarization curves in Fig. 8 compare each individual cell of the two-cell assembly against the series combination of the two, and verify additive performance using the flip-flop configuration. Fig. 9 shows the power density curve, with a peak level of about 20 mW/cm^2, normalized by the fact that there are two cells. Interestingly, the overall performance of the interconnected run was slightly higher than each of the single cells operating separately. Presently there is no clear evidence confirming that this type of series connection would exhibit synergistic phenomena, so membrane conditioning (e.g. self-humidification) stands as the most plausible explanation.

Whether the net effect is synergistic or parasitic, the fact that two cells share one common membrane raises the

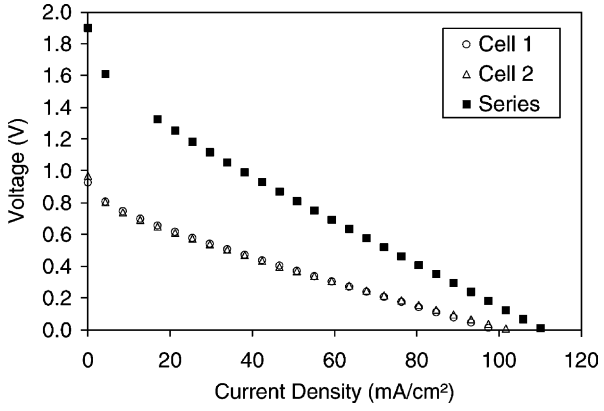

Fig. 8. Polarization curves of two-cell assembly. The flip-flop series interconnection does in fact provide the voltage sum of each of its individual cells.

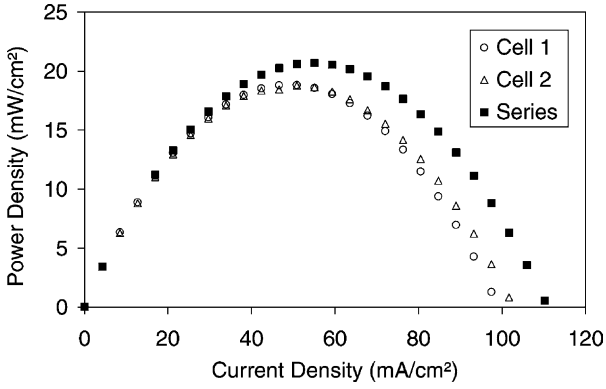

Fig. 9. Power density of two-cell assembly. Notably the series combination of two cells together showed slightly higher performance than the sum of each of its parts.

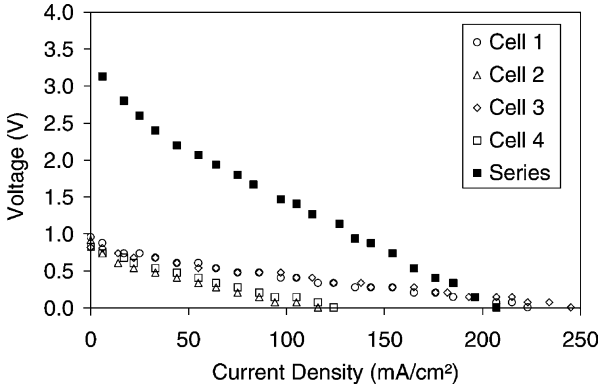

Fig. 11. Polarization curves of four-cell assembly. The series interconnection does provide the voltage sum of each of its individual cells. However, the four individual cells do not exhibit uniform behavior.

question of ion "cross-conduction" laterally between the cells, rather than perpendicular to the membrane as intended. The distance separating the two cells was 8 mm, which is large compared to the 125 μm thickness of the membrane, so it was not expected that any cross-conduction would occur. However, as a confirmation experiment, a discontinuous two-piece MEA was compared to the continuous membrane. Both MEAs were originally identical with two electrode pairs on one membrane, but in the latter case the membrane was severed. Fig. 10 shows that the performance is nearly identical, leading to the conclusion that there is no appreciable current in the lateral direction for this particular prototype configuration. The small difference in slope of the current–voltage curve (indicating Ohmic loss) may be attributed to imperfect repeatability of clamping force and hence some variability with respect to contact resistance. Preliminary trials using closer array spacing, however, have shown evidence that does suggest some parasitic cross-conduction among neighboring cells, and more dedicated treatment of this phenomena will be presented independently in a related paper.

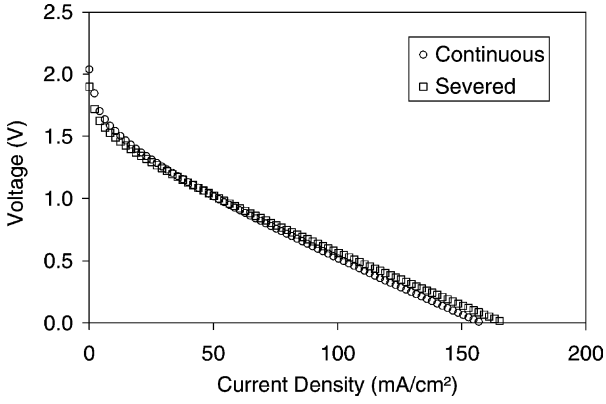

Fig. 10. Comparison of continuous vs. severed membrane. The performance is not affected by whether or not the shared membrane is continuous or severed, suggesting that the system does not exhibit significant lateral cross-conduction through the membrane.

4.1.2. Four-cell assembly

Fig. 11 compares the series assembly of four cells against each one operating separately. As seen in the two-cell case, the overall assembly produces voltage output equal to the sum of the four unit cells. The overall series assembly achieved a maximum power density of 42 mW/cm^2 (total power divided by the summed area of the four 1 cm^2 cells).

Although the open-cell voltage was nearly identical for all cells, the four-cell assembly revealed non-uniformity that was not observed in the two-cell case. Clearly two of the cells (cells 2 and 4) showed weaker performance than the other two (cells 1 and 3). The test apparatus was designed such that the gold contact for each cell had approximately equal distance to the point of external probe measurement. Therefore, the path length of electrical conduction was not considered to be a significant factor. Closer investigation,

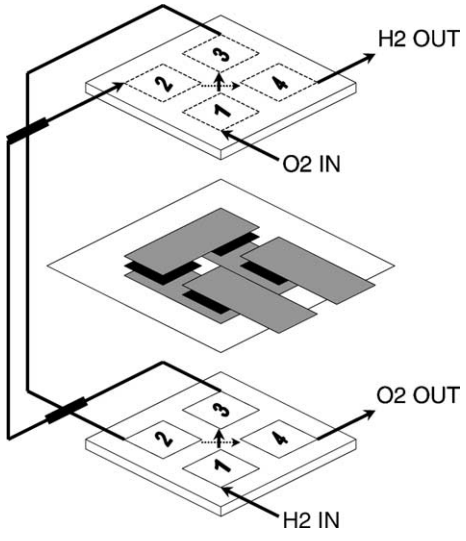

Fig. 12. Gas distribution path for four-cell assembly. The hydrogen path is bottom-1, bottom-3, top-2, top-4, and the oxygen path is top-1, top-3, bottom-2, bottom-4. The cross-channels at the center were etched on different levels of the wafer, so there is no mixing of gases as they cross-diagonally across the array.

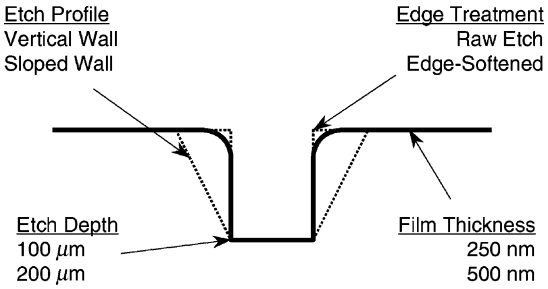

Fig. 13. Experimental factors for thin-film conduction over channel topology. Test samples were fabricated under the full factorial set of conditions, and resistance across the trench was measured to quantify the factor effects.

however, revealed a correlation between the individual cell performance and the position of the cell along the gas distribution path. Fig. 12 shows that cells 1 and 3 were supplied with reactant gases closest to the inlet. The downstream cells are, therefore, more likely to suffer from pressure loss, reactant depletion and water management problems. Correspondingly, cells 2 and 4 demonstrated lower individual performance.

4.2. Etch profile considerations for metal film conduction

Vapor deposition of metal film showed success in providing current collection for the etched glass and silicon flow structures. For miniature fuel cells, such methods are highly favorable for selective patterning as well as parallel manufacturing. However, electrical resistance in the films, especially over varying etch topology is a fundamental concern for high performance. Therefore, a follow-up study was conducted to quantitatively understand factor effects of the relevant design parameters. Factorial design methods [16,17] were applied to investigate how etch profiles influence resistance across conformal thin-film metal. Fig. 13 describes the four factors that were studied, as well as the specific levels for each. The resistance was measured along the conformal surface by placing probe contacts on the horizontal surfaces at opposite sides of the trench.

Table 1
Factorial experiment results for resistance across conformal thin-film metal

	Profile	Depth (μm)	Corner	Thickness (nm)	Average ($N = 8$)	S.D.
1	Rectangle	100	Raw	250	0.490	0.0207
2	Rectangle	100	Raw	500	0.268	0.0121
3	Rectangle	100	Smooth	250	0.447	0.0165
4	Rectangle	100	Smooth	500	0.236	0.0044
5	Rectangle	200	Raw	250	0.546	0.0267
6	Rectangle	200	Raw	500	0.274	0.0107
7	Rectangle	200	Smooth	250	0.508	0.0048
8	Rectangle	200	Smooth	500	0.261	0.0059
9	Trapezoid	100	Raw	250	0.450	0.0187
10	Trapezoid	100	Raw	500	0.243	0.0054
11	Trapezoid	100	Smooth	250	0.415	0.0048
12	Trapezoid	100	Smooth	500	0.222	0.0045
13	Trapezoid	200	Raw	250	0.431	0.0064
14	Trapezoid	200	Raw	500	0.239	0.0053
15	Trapezoid	200	Smooth	250	0.424	0.0066
16	Trapezoid	200	Smooth	500	0.240	0.0057

All test samples were etched in silicon wafers, where the particular profile was determined by etch method. An isotropic plasma etch (as described previously) provided straight sidewalls, while anisotropic wet etching in potassium hydroxide resulted in 54.7° sloped walls according to silicon crystal planes. Etch depth and film thickness were both controlled by process time. Softened edges were created by 1 min immersion of samples in a caustic solution selected for preferential etching of sharp corners (1:2:1 mixture of 49% hydrofluoric acid, nitric acid and 69.5% acetic acid).

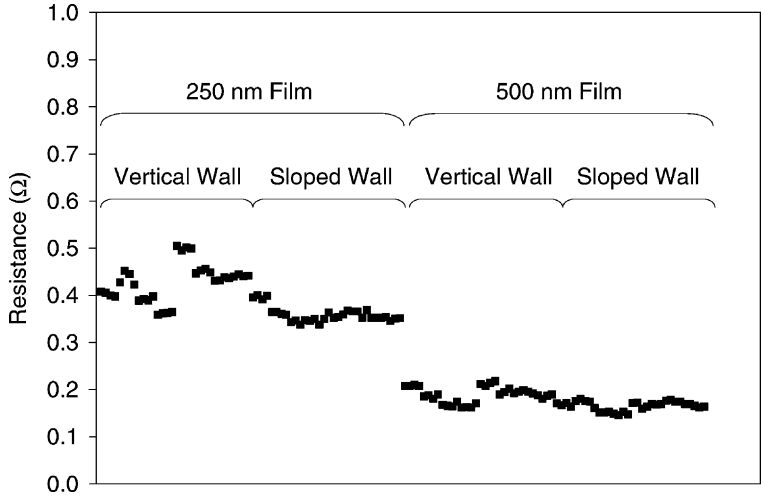

Fig. 14. Experimental results for resistance as a function of geometric etch parameters. The scatter data is grouped by dominant factors, showing that film thickness has the most significant effect. Grouping of weaker factors is not shown.

Resistance was measured with a digital Agilent multimeter having 1 mΩ resolution. The trench width was 2 mm wide and probe contacts were made on the upper plateau surfaces 1 mm away from each corner. Eight independent measurements were recorded on different samples for each of the 16 run conditions, to compensate for probe placement accuracy, contact force and potential non-uniformity across the substrate wafer. Table 1 presents the experimental data, with resistance values expressed in Ω.

The sorted scatter plot in Fig. 14 graphically shows that film thickness is clearly the dominant factor. Calculated factor effects [16] quantitatively confirm this observation as follows: etch profile, 23 mΩ; etch depth, 10 mΩ; corner treatment, 12 mΩ; and film thickness, 108 mΩ. One observation is that the absolute resistance is not prohibitively high. A more interesting revelation is that film thickness can compensate for more aggressive channel designs. For example, the ''real estate'' utilization of features using dry etching is far better than wet etching because less volume is wasted as non-functional bulk material. Even though the associated vertical walls and sharp corners are a concern for electrical resistance, a sufficiently thick film can avoid these bottlenecks. Furthermore, the relative insensitivity of resistance to etch depth makes it possible to independently optimize fluid mechanics, without being hindered by electrical design constraints.

5. Conclusions

Lateral planar interconnection offers extended possibilities for both form and function of fuel cells, but miniaturization introduces new design challenges beyond those of traditional fuel cell stacks. The ''flip-flop'' interconnection scheme overcomes some difficult engineering challenges by working with a fully continuous membrane. Advantages include simplifications in membrane processing and interconnect design. There is an associated trade-off with the need to alternate reactant cavities within a single backing structure, but wafer-level packaging for miniature cells offers promising solutions.

Multiple prototypes with the ''flip-flop'' series design have been developed and the systems have successfully confirmed additive performance. A variety of etching and deposition techniques adopted from microfabrication have been applied to glass and silicon substrates in two-cell and four-cell configurations. Microfabrication presents a well-integrated and parallel manufacturing approach, mimicking the paradigm of integrated circuits. Current collection was successfully achieved by patterning metal films on an insulating substrate, and factorial experimentation has concluded that film thickness is the dominant factor compared to other parameters related to channel topology.

The prototypes have demonstrated appreciable power density in excess of 40 mW/cm^2, even without the high mechanical compression required by larger stacks. Experience with the prototypes has uncovered potential topics for future study, including a concern over lateral ionic conduction within the membrane as well as the effects of non-uniform reactant distribution over a largely planar network.

Acknowledgements

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